AMATEUR RADIO RESEARCH AND DEVELOPMENT CORPORATION (AMRAD)

VADCG TERMINAL NODE CONTROLLER (TNC)
DAUGHTER BOARD VDS-1

INSTRUCTION MANUAL

JULY 1, 1984

NOTICE NOTICE NOTICE

Amateur Radio Research and Development (AMRAD) is a not-for-profit organization, incorporated in the State of Virginia. AMRAD is dedicated to the advancement of the state-of-the-art of Amateur Radio communications. This board was designed by AMRAD and Terry Fox, WB4JFI to allow the continuation of the use of the Vancouver Amateur Digital Communications Group (V.A.D.C.G.) Terminal Node Controller (TNC). This board is sold as a retrofit subsystem to the VADCG TNC, and as such, no warranties are expressed or implied, either for its proper operation, or the proper operation of the host TNC board.

It is requested that all users of this board support AMRAD by joining this organization. That way all users will receive the AMRAD Newsletter, which will contain updates, corrections, and enhancements to the VDS-1, along with a wealth of other information regarding packet radio, and Amateur Radio in general.

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CIRCUIT FEATURES

Recently, The Amateur Radio Research and Development Corporation (AMRAD), originators of the now popular AX.25 packet radio protocol, developed a retrofit board for the Vancouver Terminal Node Controller board, originally developed by Douglas Lockhart, VE7APU. Using the daughter board (part number VDS-1), systems designers are now freed from the memory constraints of the original board. This translates into better operation for the Vancouver TNC packet radio enthusiast.

Some of the advantages of the AMRAD Vancouver Daughter board system are:

* No modifications (jumpers or traces cut) required on the Vancouver board for normal operation
* No jumper wires to hook between the two boards. All connections necessary are done via wire-wrap sockets.
* From 8k (using 2716's) to 32k (using 2764's) of EPROM
* From 8k (using 6116's) to 32k (using 8k by 8 chips) of RAM
* Software programmable baud rate generator (using Intel 8253)
* Optional use of timed interrupts for better software control (requires cutting two traces on the TNC board)
* Position for up to six 16-pin sockets for user kludging
* Position for one 24-pin socket for user kludging
* General kludge area of 11 by 17 tenth-inch spaced holes
* Uses only two additional IC's (other than RAM and EPROM)
* requires no additional power supplies (in fact the minus five volt supply needed for the 2708's can be eliminated)
* Full documentation available.
* Priced inexpensively at only $25.00 for the bare board. (which is a Mil-Spec quality board)

To order a VDS-1 board, send $25.00 Plus $2.25 for shipping (US funds) to:

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VANCOUVER TNC BOARD CHANGES

It is not necessary to make any changes to the Vancouver TNC board unless one or more of the following is true:

1. Use of timed interrupts from the 8253 are planned.

2. The VADCG TNC board was originally assembled using IC sockets with small holes. Since the VDS-1 interfaces to the VADCG TNC through wire-wrap sockets plugged into four key sockets (U1, U9, U11, and U18) on the TNC, these sockets must be capable of accepting the larger pins that wire-wrap sockets have. If this is not the case, the offending socket(s) must be replaced with ones that will work before using the VDS-1.

These changes to the VADCG TNC are easily accomplished if necessary, and will not affect the operation of the TNC with or without the VDS-1 installed.

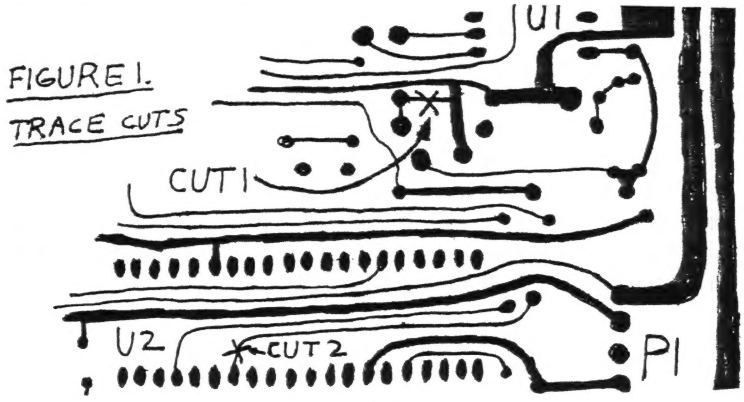
1. Allowing Timed Interrupts From The VDS-1 8253.

The Intel 8253 timer chip contains three indepentently programmable timers. One of these is used to provide software control of the packet channel baud rate. The other two are available to the programmer to provide timed interrupts to the TNC. Timer 1 is optionally wired to the non-maskable Trap interrupt input pin of the 8085 CPU, while timer 2 is optionally wired to the maskable INTR interrupt pin of the 8085 CPU.

Unfortunately, the VADCG TNC has both of these pins shorted directly to ground (in addition to having pull-down resistors). In order to use these inputs to the CPU, they must first be disconnected from ground. This is accomplished by cutting two traces on the TNC board.

The trace that must be cut to allow the Trap interrupt is located on the bottom of the TNC board, near pin 1 of the 8085 CPU (U1). See Figure 1, Cut 1, for the exact location to place the cut.

Figure 1 also shows the position of the trace that must be cut to allow the INTR to be used. It is located by pin 14 of U2, the 8255 Parallel Port IC. Cut the board as shown by Cut 2.



2. TNC Socket Changes

As previously mentioned, certain sockets (U1, U9, U11, and U18)on the TNC board MUST be able to accept the larger pins used on wire-wrap IC sockets.

If any of the sockets won't accept the wire-wrap socket pins, change the socket in question. This can be a lot easier than it sounds, using the following technique.

STEP 1 Remove the IC in the socket to be changed.

STEP 2 Turn the board over (component side down), and locate the socket in question. Using a solder-sucker (or solder wick) and a low-wattage soldering iron, carefully remove as much of the solder as possible on each pin. The more solder removed on each pin, the better, but don't spend a lot of time on each pin, or the trace may come loose from the board. After all the pins have been hit once, look over each pin, and try once again to remove any remaining solder. At this point, you should be able to see through the holes at least most of the sockets pins.

STEP 3 Using a small pair of needle-nose pliers, heat each pin with the soldering iron, and wiggle that pin with the pliers. Keep wiggling the pin as you remove the soldering iron and the pin cools down. If the solder was sufficiently removed in the last step, the pin should stay loose in the hole after the pin cools down. Do this with each pin on the socket. Don't worry if all the pins don't become loose at first, as long as most are.

STEP 4 Turn the TNC board over. Carefully pry a very small bladed screwdriver between the PC board and the IC socket. Be careful not to scratch the board while doing this. Remember, the socket you are removing is to be thrown away, so scratch it if necessary rather than the TNC board. While prying the socket away from the board, heat up any socket pins that may still be soldered to the board. By alternating the heat between any pins that are still soldered and carefully prying with the screwdriver, the socket should be walked out of the PC board holes.

STEP 5 Once the socket has been removed, go over the holes on the TNC PC board with solder wick to remove any solder left behind.

STEP 6 Place the new socket on the TNC board, and solder it in place. Check the new socket to be sure there are no solder bridges. It is a good practice to re-install the removed IC in the new socket and check the TNC for proper operation before installing the VDS-1.

VDS-1 BOARD ASSEMBLY

Use the following step-by-step instructions to properly assemble the VDS-1 daughter board. Place a check mark beside each step as it is completed.

In order to use the wire-wrap sockets as jumpers between the two boards, the holes on the daughter board were made larger than normal. This may make it harder to solder the sockets onto the board. Make sure that whenever soldering sockets to the daughter board there is sufficient solder between the PC eyelet and the socket pin. The use of a small, pointed tip on your soldering iron will help.

1. Place four 28 pin solder-tail sockets in the RAM positions (U34, U35, U36, and U37). Solder pins 1 and 15 on each socket to hold it in place. When all four sockets are in place, solder the remaining pins on the four sockets. Check for solder bridges and cold solder joints.

2. Put the following solder-tail sockets in their positions on the board and solder them in place:

   A) 16 pin socket at U38.

   B) 16 pin socket at U39.

   C) 14 pin socket at U40.

   D) 14 pin socket at U42.

   E) 24 pin socket at U41.

3. Install either four 28 pin solder-tail sockets, or four 28 pin Zero Insertion Force (ZIF) sockets at the four EPROM locations, U30, U31, U32, and U33. Solder pins 1 and 15 of each socket first, to hold the socket in place. Then solder the remaining pins. Check for solder bridges.

VDS-1 BOARD ASSEMBLY (CONTINUED)

NOTE: When installing the wire-wrap sockets in the next steps, be sure they are mounted flush to the board, and the pins are not crooked. If the sockets are not soldered down flush to the board, the pins will be crooked, causing alignment problems during board installation.

4. Install a 40 pin wire-wrap socket at U1. Notice that pin 1 is in the opposite direction as the rest of the sockets of the board. Carefully solder the wire-wrap socket to the daughter board, making sure there are no solder bridges.

5. Install a 24 pin wire-wrap socket at U18. Carefully solder it to the daughter board, making sure there are no solder bridges. Place a piece of tape over the socket, since no IC will be installed in this socket.

6. Place a 16 pin wire-wrap socket at U9. Note the placement of pin 1. Solder all pins onto the daughter board.

7. Install a 14 pin wire-wrap socket at U11, noting the placement of pin 1. Solder the socket to the board, checking for solder bridges. Place a piece of tape over this socket, since there will be no IC installed in it.

8. Install the 47 uF, 15 volt electrolytic capacitor at position C1 (next to U18) (the value of this component is very non-critical). Solder the capacitor to the board.

9. Install the six .1 uF bypass capacitors at C2 to C7 on the board, and solder them in place.

10. Before installing the VDS-1, make sure the 5 volt bus is not shorted to ground at any point by measuring the resistance between the 5 volt bus and ground with a volt-ohm-meter. It should read relatively low at first, then slowly rise to a high resistance level (depending on the value of C1).

11. If the VDS-1 passes a visual inspection, proceed to the next section of this manual (Installation and Checkout).

INSTALLATION AND CHECKOUT

This section describes how to install the VDS-1 on the VADCG TNC board. Be careful not to bend any of the wire-wrap pins out of alignment, or the board will not fit as snugly as designed. As with the VDS-1 assembly procedure, check off each step as it is completed.

1. If the VDS-1 is to be altered from its original configuration at jumper areas JP-5, JP-6, JP-7, or the 8k RAM devices are to be used, check the Option Settings section of this manual before proceeding to the next step here. Since these jumper areas are "normalled" on the back of the VDS-1, the preset jumper traces must be cut BEFORE the VDS-1 is installed onto the TNC board (except for JP-8).

2. Carefully remove the following ICs from the VADCG TNC board, making sure they are not overly handled:

   A) U1, 8085, CPU chip.

   B) U7, 74LS00, quad nand gate (part of memory decoding).

   C) U8, 74LS138, one-of-eight decoder (memory decoder).

   D) U9, 74LS138, one-of-eight decoder (port decoder).

   E) U11, CD4024, binary counter (baud rate generator). (be careful with this IC, as it is very sensitive).

   F) U15 thru U18, 2708 EPROM memory.

   G) U19 thru U26, 2114 RAM memory.

3. Carefully position the daughter board over the main TNC board, making sure not to bend any of the wire-wrap socket pins. Line up the wire-wrap pin sockets, starting with U1. Do not press the pins down into the sockets on the TNC board yet, just hold them gently in the socket holes. The daughter board has been designed very carefully to make sure that the wire-wrap pins line up properly. If there is a problem with pin alignment, one or more of the sockets may have been soldered in slightly crooked (this happened on the VDS-1 prototype). If the pins don't align properly, either the socket should be re-soldered, or the pins can be bent slightly using a pair of needle-nose pliers.

4. After U1 has been aligned, check U11 to see if the pins on the opposite end of the VDS-1 are also coming into proper alignment. If they are, look between the two boards and make sure U9 is also lined up properly. Lastly, check U18 at the top of the board for proper pin alignment. It may be necessary to move the daughter board around slightly to accomplish proper alignment on all pins of all sockets. Take the extra time to be sure all pins line up without having to stress either board, as this will help if the board ever needs to be removed and re-installed.

5. Once all the wire-wrap pins line up properly to the holes in the sockets on the VADCG TNC board, place the board on a hard, flat surface and gently press on each wire-wrap socket using the following sequence until you feel the pins bottom out in the TNC sockets below.

   A) Press the U1 socket down first, since the 40 pin socket will be the hardest to align properly.

   B) Next, press the U18 socket down, making sure the rest of the sockets are still lined up properly.

   C) Now, press the U9 socket into its socket on the TNC board.

   D) Lastly, press the U11 socket into its socket on the TNC board.

6. Make sure at least one of the switches of dip switch S-2 on the TNC board is ON. It doesn't matter which, as all the necessary pins on the U11 socket are shorted together on the VDS-1.

7. Perform one final check before installing the ICs on the daughter board, looking over the following:

   A) Make sure all the wire-wrap pins are properly lined up in their socket holes. Make sure none of the pins are bent into wrong holes, two pins are shorted together, or any of the pins are missing their holes completely.

   B) It is a good idea to take a final reading of the resistance between the five volt buses and ground, making sure there are no direct shorts. If there are, remove the VDS-1 from the TNC, and check each board separately for shorts.

7. Install the following Integrated Circuits in their sockets:

   A) 8085 CPU at U1.

   B) 74LS138 port decoder at U9.

   C) 74LS138 EPROM decoder at U38.

   D) 74LS138 RAM decoder at U39.

   E) CD4024 binary counter at U40.
   (Note that this chip seems very sensitive to static)

   F) 8253 timer at U41.

   G) RAM memory chips (minimum of 2) at U34 to U37.
   (minimum 2k parts RAM are U34 at RAM0, U35 at RAM1)

   H) EPROM's as necessary in sockets U30 through U33.
   (U30 is ROM0, address 0000H)

   I) DO NOT INSTALL U42 AT THIS TIME. It is used only for timed-interrupts, and should be left off during initial board checkout.

8. It should be noted that since the memory address has been altered to allow expanded EPROM and RAM, and since the packet channel baud rate is now controlled with software rather than S-2, new sofware must be used whenever using the VDS-1. Details on software alterations to support the VDS-1 are provided in the Software Support section of this manual.

   It is a good idea to use a monitor program to test the TNC system after installing the VDS-1. This way, any problems with packet radio code not functioning properly can be traced to software, rather than hardware. There are different monitor programs available for the TNC baord. If you cannot obtain one from a local packet enthusiast, contact AMRAD for software support (either 8080 type assembly language files under CP/M, or burned EPROMs). Note that since AMRAD is a voluntary organization, EPROMs may not be immediately available (in other words, expect the possibility of a slight delay).

Whenever requesting EPROM support from AMRAD, be sure to include all necessary information such as:

A) Station Callsign, including SSID.

B) Repeater Callsigns (including SSID's) of any repeaters to be used as a default condition during power-up.

C) Are repeaters are to be defaulted on or off at power up.

D) Terminal configuration. This includes terminal speed, parity on/off, parity type, number of stop bits, and if this TNC is to be used as a terminal or host computer. Normal operation is 1200 baud, no parity, one stop bit, and no repeaters.

E) Default packet channel baud rate at power on. This is normally set to 1200 baud.

9. Apply power to the TNC board. If all goes properly, a sign-on message should appear on the terminal. If it does, install the EPROMs containing the packet radio code, and try them out. If they function properly, your TNC board is once again ready to snatch frames from the air. Try monitoring an active packet channel for a while, and connect to someone to be sure that all of the packet functions are working properly.

10. If you board does not operate properly, using either the monitor program or the packet code, see the Troubleshooting and Theory of Operation sections of this manual.

11. If timed-interrupts are to be used, install U42 (74LS00), and apply power. Check for proper interrupt operation.

Option Settings

The VDS-1 daughter board is designed to be flexible in the type and amount of RAM and EPROM it will support. It will also allow the timed-interrupts and packet channel baud rate to be programmed under software control. There are several jumper areas provided on the board for alteration of the standard configuration. Each of these options, their associated jumper locations, and default settings will be discussed here.

EPROM TYPE **DEFAULT TYPE 2732**

The VDS-1 is designed to use 2716, 2732, or 2764 type EPROMs. To alter the VDS-1 from the default 2732 type, jumper JP-5 must be changed. Use the following steps to alter JP-5:

1. Turn the VDS-1 board over and locate JP-5 (next to the 74LS138 EPROM decoder, U38). Notice that there are PC traces between several pins of JP-5 that are slightly thinner than most of the others in that area of the board. Using an Xacto knife, carefully cut the following traces between the two pins of JP-5 as listed:

   A) Cut trace between JP-5 pins 1 and 14.

   B) Cut trace between JP-5 pins 2 and 13.

   C) Cut trace between JP-5 pins 3 and 12.

   D) Cut trace between JP-5 pins 4 and 11.

   Install a 14 pin solder-tail socket at JP-5 and solder it in place.

   Configure a 14 pin DIP header for the proper type of EPROM memory chips as follows:

   A) 2716 type EPROMs. Wire the following pins together:

      Pin 4 to pin 14 (Address line A11 to U38 address A0).
      Pin 1 to pin 13 (Address line A12 to U38 address A1).
      Pin 2 to pin 12 (Address line A13 to U38 address A2).
      Pin 10 to pin 11 (+5 volts to 2716 pin 23).

   B) 2732 type EPROMs. Wire the following pins together:

      Pin 1 to pin 14 (Address line A12 to U38 address A0).
      Pin 2 to pin 13 (Address line A13 to U38 address A1).
      Pin 3 to pin 12 (Address line A14 to U38 address A2).
      Pin 4 to pin 11 (Address line A11 to 2732 A11).

C) 2764 type EPROMs. Wire the following pins together:

Pin 2 to pin 14 (Address line A13 to U38 address A0).
Pin 3 to pin 13 (Address line A14 to U38 address A1).
Pin 5 to pin 12 (Address line A15 to U38 address A2).
Pin 4 to pin 11 (Address line A11 to 2764 A11).

Install the DIP header in the socket located at JP-5. The resulting memory maps are as follows:

A) 2716 EPROM memory map:

0000H-07FFH	U30 (EPROM 0).
0800H-0FFFH	U31 (EPROM 1).
1000H-17FFH	U32 (EPROM 2).
1800H-1FFFH	U33 (EPROM 3).

B) Default 2732 EPROM memory map:

0000H-0FFFH	U30 (EPROM 0).
1000H-1FFFH	U31 (EPROM 1).
2000H-2FFFH	U32 (EPROM 2).
3000H-3FFFH	U33 (EPROM 3).

C) 2764 EPROM memory map:

0000H-1FFFH	U30 (EPROM 0).
2000H-3FFFH	U31 (EPROM 1).
4000H-5FFFH	U32 (EPROM 2).
6000H-7FFFH	U33 (EPROM 3).

RAM TYPE **DEFAULT: 6116 TYPE**

If the RAM memory chips used are to be changed from the default 6116 type devices, use the following procedure:

1. Turn the VDS-1 board over to the bottom of the board (COPYRIGHT 1984 notice) and locate JP-6 (next to U39). Locate and cut the following traces at JP-6:

   A) Cut trace between JP-6 pins 1 and 14.

   B) Cut trace between JP-6 pins 2 and 13.

   C) Cut trace between JP-6 pins 3 and 12.

   D) Cut trace between JP-6 pins 6 and 9.

2. Install a 14 pin solder-tail socket at location JP-6, and solder it in place.

3. Wire a DIP header for the type of RAM memory to be used according to the following:

   A) If 6116 type (2k by 8) devices are being used:

      1) Wire pin 1 to pin 14 (Address line A11 to U39 A0).

      2) Wire pin 2 to pin 13 (Address line A12 to U39 A1).

      3) Wire pin 3 to pin 12 (Address line A13 to U39 A2).

      4) Wire pin 6 to pin 9 (WR* to 6116 WR* pin).

   B) If 6264 or 2186 RAM chips (8k by 8) are being used:

      1) Wire pin 3 to pin 14 (Address line A13 to U39 A0).

      2) Wire pin 4 to pin 13 (Address line A14 to U39 A1).

      3) Wire pin 5 to pin 12 (Address line A15 to U39 A2).

      4) Wire pin 1 to pin 9 (Address line A11 to RAM A11).

4. Place the appropriate DIP header into the socket at JP-6.

5. If 2186 RAM chips are being used, also install jumpers at locations JP-9, JP-10, JP-11, and JP-12 on the BOTTOM of the VDS-1 board. The 2186 type RAM chips are actually psuedo-static devices, which may require synchronization with the 8085 CPU. These jumpers hook the 2186 ready lines to the 8085 ready pin, allowing memory synchronization.

6. The resulting memory map for the RAM memory is:

   A) For 6116 type (2k by 8) devices:

8000H-87FFH	U34	(RAM 0)
8800H-8FFFH	U35	(RAM 1)
9000H-97FFH	U36	(RAM 2)
9800H-9FFFH	U37	(RAM 3)

   B) For 6264 and 2186 type (8k by 8) devices:

8000H-9FFFH	U34	(RAM 0)
A000H-BFFFH	U35	(RAM 1)
C000H-DFFFH	U36	(RAM 2)
E000H-FFFFH	U37	(RAM 3)

TIMER OPTIONS

There are three independent, software programmable timers in the 8253 timer IC. The only timer that must be used in support of the VDS-1 daughter board is timer 0, which is used to generate the baud rate of the packet channel. For proper operation, the 8253 input clock cannot exceed 2 MHz. Unfortunately, the Vancouver TNC master clock frequency is 2.4576 MHz. This means the master clock must be divided before sending it to any of the clock inputs of the 8253.

In addition, since the maximum divisor of a sixteen bit counter is 65,535 and the input clock would now be 1.2288 MHz, the slowest resulting interrupts would be about 19 per second, with no trim control in that range (next slowest would be double that, or 38 interrupts/sec.). There needs to be a better way of trimming the number if interrupts per second, if timed-interrupts are to be used effectively. This is accomplished with U40 and JP-7.

The outputs of U40 (CD4024) are wired to pins 1, and 3 thru 7 of JP-7. Each of these pins is a successive divide-by-two of the previous pin's frequency. The following pins at JP-7 have the accompanying frequencies, and are normally jumpered to the following input clocks of U41:

Pin 1	1.2288 MHz	(Baud Rate Generator input)
Pin 3	6144 KHz	(Trap timer, INTR timer inputs)
Pin 4	3072 KHz	
Pin 5	1536 KHz	
Pin 6	768 KHz	
Pin 7	384 KHz	

Pin 14 of JP-7 is normally jumpered to the input clock of timer 0 in U41. This provides an acceptable clock frequency to timer 0, which is used as the baud rate generator for the packet channel. Other outputs could be used if necessary, but the need for this is not anticipated.

Pin 13 of JP-7 is the input clock to timer 1 of U41. Timer 1 optionally drives the Trap interrupt input to the 8085 CPU. The trap interrupt is non-maskable, so there is no way of disabling these interrupts if the hardware is enabled. Using the second output of U40 usually gives enough control of the resulting interrupt rate.

Pin 12 of JP-7 is the input clock to timer 2, and is also normally wired to the second output of U40. Timer 2 optionally drives the INTR interrupt input to the 8085 CPU. The INTR pin generates a maskable interrupt, which allows the software to selectively disable this interrupt. As with the Trap interrupt above, the second output of U40 usually gives enough control over the frequency of INTR interrupts.

If any of the timing parameters set by JP-7 are to be altered, it is recommended that a socket be installed at JP-7, and DIP headers be used to change the default values. This is accomplished as follows:

1. Turn the VDS-1 board over and locate jumoer JP-7 (next to the U40 socket). Carefully cut the following traces:

   A) Pin 1 to pin 14

   B) Pin 2 to pin 13

   C) Pin 2 to pin 12

2. Place a 14 pin solder-tail socket at JP-7, and solder it in place.

3. Wire a DIP header as necessary for the alterations requied.

4. Place the DIP header in the socket at JP-7, and test out the changes.

TIMED INTERRUPT ENABLES

The output of the two timers that are capabe of generating interrupts are normally disabled by not installing U42 (74LS00). If timed interrupts are to be used, U42 should be installed. Jumper JP-8 is used to selectively enable only one or the other of the timed interrupts, as necessary. JP-8 is normally jumpered on for both interrupts. other configurations can be made by cutting the traces ot the TOP of the board at JP-8 as follows:

1. Cut trace between pins 1 and 4 to disable Trap interrupts.

2. Cut trace between pins 2 and 3 to disable INTR interrupts.

These traces were placed on the TOP of the VDS-1 board to allow easy access to them.

Keep in mind that the timers MUST be properly programmed before timed interrupts are enabled, otherwise improper operation will result. Note that timers 1 and 2 should be programmed for pulse operation, rather than square wave, since the interrupts are level sensitive.

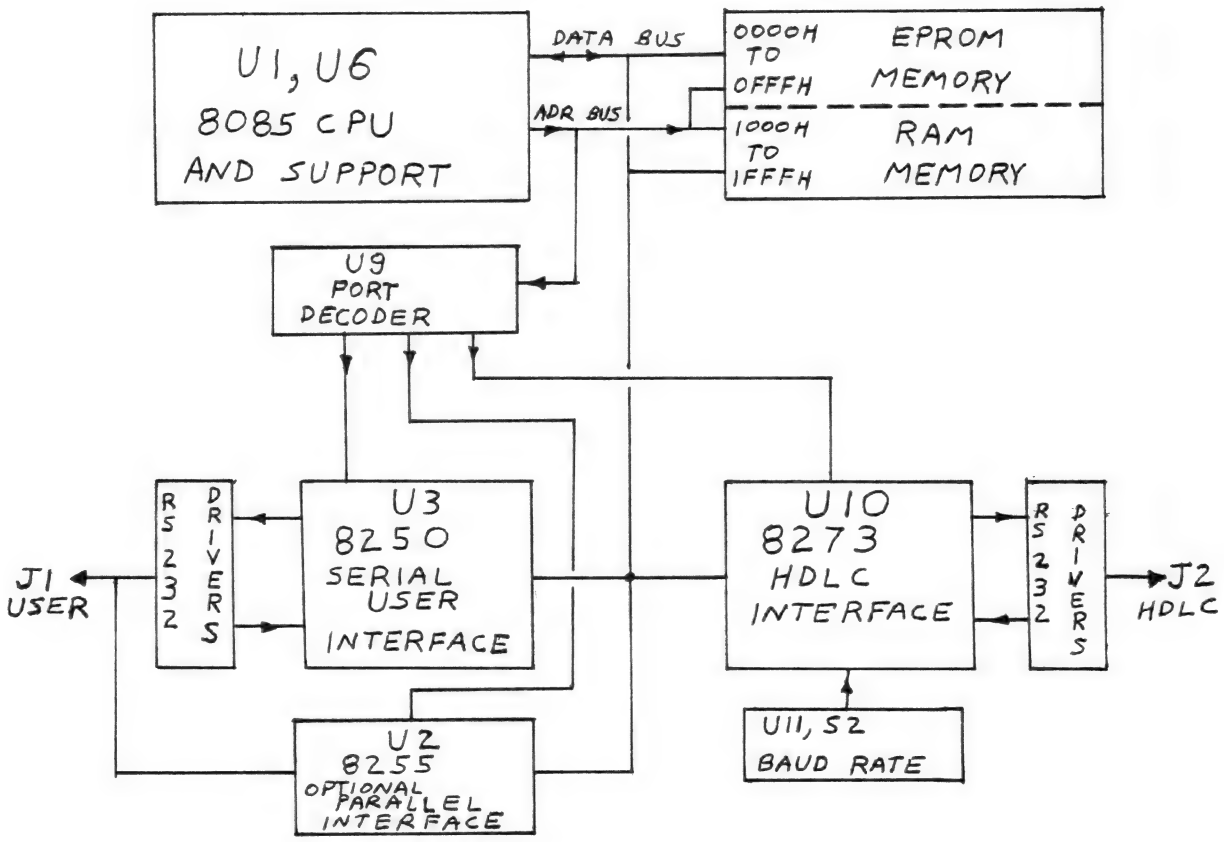
THEORY OF OPERATION

In order to better understand how the VDS-1 daughter board interfaces with the VADCG TNC, we will first delve into the VADCG TNC itself. Since the original manual supplied with the VADCG TNC did not contain a theory of operation section, we will try to fill in that gap to some degree here.

TNC HARDWARE OVERVIEW

The VADCG TNC is actually a single board computer dedicated to changing data between two different transmission formats (usually asynchronous ASCII and HDLC type frames). Like most other single board computers, the TNC has a Central Processing Unit (CPU) that acts as the brains of the computer, EPROM memory that contains the instructions for the CPU, RAM memory to hold data and control information temporarily, and some input and output (I/O) devices with which to communicate to the outside world. See Figure 2 for a block diagram of the VADCG TNC.

FIGURE 2. TNC BLOCK DIAGRAM



CPU AND AND CPU SUPPORT CIRCUITRY

The VADCG TNC board uses the Intel 8085 CPU chip. The 8085 is an improved version of the popular 8080. It is software compatible with the 8080, which means programs written for the 8080 will usually run fine on an 8085.

The 8085 CPU has a built-in clock generator. On the VADCG TNC board, a 4.9152 MHz crystal is used to determine the clock rate. This frequency was probably chosen because it is a multiple of most of the standard baud rates. The internal oscillator divides this frequency in half, resulting in an actual clock rate of 2.4576 MHz (both internal to the 8085 and the rest of the board).

The 8085 uses a multiplexed data and low half address bus. This means that the data and lower portion of the addresses share the same set of pins on the 8085. In order to accomplish this, the 8085 sends a special signal out, called Address Latch Enable, or ALE, whenever address information is on the AD0-AD7 lines. On the TNC board, an eight-bit latch (U6, 74LS373) is used to latch and hold the low address whenever told to by the ALE pin from the 8085.

The 8085 CPU has several pins that can be used to directly control the CPU actions. Some of these are the same as the 8080, while others are new to the 8085.

The reset pin causes the CPU to stop whatever it was doing, and immediately go to the beginning of memory. This pin should be hooked to a pushbutton type switch so that the operator can recover the board in case of a failure in program control.

There are several interrupt pins on the 8085. Interrupts are just what the name implies, if the associated pin is asserted, the CPU will temporarily suspend whatever it is doing, and do something else (whatever the interrupt requested, or the CPU is programmed to do). Some interrupts are controllable (maskable) as to whether the CPU will acknowledge and honor them, while others the CPU has no control over (non-maskable), in which case the CPU MUST honor the interrupt. Since there are several different interrupts, and each may occur at any time, each one is assigned an order of precedence. The interrupts on the TNC baord will be discussed in increasing order of importance.

The lowest priority interrupt is the INTR pin on the 8085 (pin 10). This pin is level sensitive, a high indicates a request for interrupt. It is maskable, allowing the CPU to ignore any INTR requests. If an INTR interrupt is allowed by the CPU, the CPU will indicate this by asserting the Interrupt Acknowledge pin (INTA*) low. The requesting device can then force an instruction (usually a call or restart) onto the data bus, and the CPU will excute that instruction. The VADCG TNC normally has this pin tied low, disabling the INTR function.

The next group of interrupts are the RST pins. These pins have a higher priority than the INTR pin, are maskable by the CPU, but they operate slightly differently. When one of the RST pins is asserted, it causes the CPU to go to a specific location in memory, and execute instructions starting at that location as if a call to that location was requested. The memory location called, the type of signal used, the order of priority, and source of the request on the TNC board are shown below.

Interrupt	Memory	Signal	Priority	Interrupt Source
RST 5.5	002CH	High	Low	User Interface
RST 6.5	0034H	High	Middle	U10 (8273) TxINT
RST 7.5	003CH	Pulse	High	U10 (8273) RxINT

The highest priority interrupt on the 8085 is the Trap interrupt (pin 6). It is non-maskable, and generates a restart to memory location 0024H. It is both edge and level sentitive. The TNC board has this pin tied low, disabling the Trap interrupt.

The 8085 CPU also generates some timing signals needed for proper computer operation. These include:

IO/M* Low for memory request, high for input/output
RD* Low indicated a read function from memory or I/O
WR* Low indicates a write function to memory or I/O
RESET OUT High indicates the CPU is being reset.

There is also a pin called Ready, which is used to synchronize CPU operation with slower memory. This pin is not used on the original VADCG TNC board.

TNC EPROM MEMORY

In order for the TNC board to function properly, the CPU must be told what to do by a program. This program is held in Erasable-Programmable-Read-Only-Memory (EPROM). The TNC uses four 2708 type EPROM chips, each of which holds 1024 bytes of program, for a total of 4096 bytes (4k) of program memory.

There is a memory decoder circuit made up of U7 (74LS00) and U8 (74LS138) that determines where in the CPU memory the EPROM (and RAM, since the same decoder is used for both) is to reside.

The memory map for an unmodified TNC board is:

0000H-03FFH	U15 (EPROM 0)
0400H-07FFH	U16 (EPROM 1)
0800H-0BFFH	U17 (EPROM 2)
0C00H-0FFFH	U18 (EPROM 3)
1000H-13FFH	U19, U20 (RAM 0)
1400H-17FFH	U21, U22 (RAM 1)
1800H-1BFFH	U23, U24 (RAM 2)
1C00H-1FFFH	U25, U26 (RAM 3)
2000H-FFFFH	Unused, copies of above map

The 74LS00 (U7) is used with the address decoder, a 74LS138 (U8), to decode memory read-only cycles for the EPROM, and memory read/write cycles for the RAM memory.

Note that the EPROM chips are in the opposite sequence than one would assume, that is EPROM 0 is the right-most, not the left-most EPROM. The 2708 EPROMs require +5V, -5V, and +12V to operate properly.

TNC RAM MEMORY

For the TNC to function properly, in addition to EPROM memory to store the program, there must also be some amount of temporary memory that will be used to store the data it needs to process. The TNC board uses 2114 type RAM chips, which are 1024 by 4 bits. Two of these chips are needed to store a complete 8 bits worth of data. There is room for four banks of these chips, for a total of 4096 bytes of data storage. The RAM memory shares the same memory decoder circuitry with the EPROM, and is discussed above.

Since the 8085 CPU uses a bidirectional data bus, the IN/OUT pins of the 2114 chips are connected directly to the CPU data bus.

TNC INPUT/OUTPUT

In order for the TNC board to function, it must get data from the outside world to process, and then send the processed data back to the outside world when done. This function is provided by the input and output devices on the TNC board. There are two different "channels" for data to transfer between the TNC and devices connected to it. The first is the "user interface", and the second is the link or packet channel. Each one of these channels is connected to the TNC CPU through special ICs, which occupy certain port locations in the CPU port address space. Each of these ICs is also capable of generating interrupts to the CPU when it needs to be serviced.

The I/O ports used are decoded by U9, a 74LS138. It decodes only I/O port addresses, which are mapped as follows:

00H-07H	U3	8250 Serial I/O Port (User Interface)
08H-0FH	U2	8255 Parallel I/O Port (User Interface-Optional)
10H-17H	U10	8273 HDLC Protocol Main Ports (Packet Channel)
18H-1FH	U10	8273 HDLC Protocol TX Data Port (Packet Channel)
20H-27H	U10	8273 HDLC Protocol RX Data Port (Packet Channel)
28H-FFH	Unused.	

The user interfaces to the VADCG TNC board either through a serial (RS-232 or current loop) or a parallel port. Most of the software support for the VADCG TNC uses only the serial interface option, and then only an ASCII, RS-232 type of serial interface. It would have been nice to have been able to use both the serial and parallel chips simultaneously, but since they share quite a few of the same DB-25 connector pins, this is impractical without cutting several traces, and adding another connector.

Serial User Interface

The serial user interface uses an 8250 Asynchronous Communications Element (ACE). This chip has both a UART and a baud rate generator built into it. In addition to serial data lines in and out, it also provides some of the handshaking lines typically found in an RS-232 interface (DSR, DTR, RTS, CTS, DCD, and RI). The TNC board has RS-232 driver chips on it to optionally make these signals either TTL or RS-232 voltage levels. Since the ACE chip is a complicated device, several I/O ports are assigned to it for proper programming and operation.

These ports are designated as follows:

Port 00 Transmit/Receive Data Buffer Registers.
Port 01 Interrupt Enable Register (Write Only).
Port 02 Interrupt Identification Register (Read Only).
Port 03 Line Control Register (UART Functions).
Port 04 Modem Control Register.
Port 05 Line Status Register (UART Status).
Port 06 Modem Status Register.
Port 07 Baud Rate Divisor Latch Registers.

Parallel User Interface

The parallel user interface uses an 8255 Programmable Peripheral Interface (PPI). This device has 24 lines of parallel data, each of which is programmable to be either inputs or outputs. In addition, some of these lines become handshaking lines when programmed properly, allowing a full 16 bit parallel Input/Output system with complete strobing and acknowledgements.

The 24 lines of the 8255 are organized as three groups of 8 lines (groups A, B, and C), with third group (C) being further divided into two 4-bit subgroups. The programming of this chip is beyond the scope of this manual, however the Port map for this device on the TNC is as follows:

Port 08H Port A Data Bus.
Port 09H Port B Data Bus
Port 0AH Port C Data Bus.
Port 0BH PPI Control Port.
Ports 0CH-0FH will be in same as above.

Since virtually no one is using the parallel user interface, these locations are generally ignored.

Packet Channel Interface

The packet channel interface is handled by an Intel 8273 HDLC Protocol Controller chip. The 8273 is very complicated inside, in that it automatically handles a lot of the HDLC protocol functions, such as clock recovery, NRZI encoding/decoding, zero bit insertion/removal, and frame-check-sequence (CRC) generation/checking. Since the packet channel sends HDLC frames in synchronous mode (no start or stop bits) once this chip starts sending a frame of data, it must continue until all the data of that frame is sent. There can be no starting and stopping in the middle of sending a frame. This means the 8273 must be capable of getting the attention of the TNC CPU quickly whenever a frame is being sent or received.

Because of this, the 8273 uses the highest interrupts on the TNC board. The transmit and receive data registers also use separate ports than the rest of the 8273. The port map of the 8273 is:

10H 8273 Main Command/Status Register.
11H 8273 Parameter/Result Register.
12H 8273 Reset/Tx Interrupt Result Register.
13H 8273 Rx Interrupt Result Register.
14H-17H Same registers as above.
18H-1FH 8273 Transmit Data Register.
20H-27H 8273 Receive Data Register.

The 8273 does not have an internal baud rate generator, so an external divider must be used. U11, a CD4024 seven stage binary counter is used to divide down the 2.4576MHz clock to the frequencies necessary for the 8273 to work. The 8273 has a digital phase-lock-loop (DPLL) that is used to recover the data timing on the packet channel. This DPLL needs a X32 clock to function properly. The outputs of U11 are sent to switch S2. Only one of the switches on S2 should be on at any given time. The outputs of U11 provide for baud rates from 38,400 baud to 600 baud.

The 8273 provides most of the primary signals used in an RS-232 interface (TXD, RXD, CTS, RTS, and DCD). In addition, there are two each user programmable input and output pins. The VADCG TNC feeds these signals to a 14 pin DIP socket at J4. The other half of J4 leads to the RS-232 level converter ICs, which then lead to the packet channel DB-25, J2.

Daughter Board Theory

The VDS-1 daughter board was designed to replace the memory of the Vancouver TNC board. In addition, it provides software control over the packet channel baud rate, and the option of time generated interrupts.

The VDS-1 interfaces to the Vancouver TNC through four wire-wrap sockets that plug into key sockets on the TNC board. The first one is at the CPU socket, U1. The 8085 CPU now plugs into the wire-wrap socket on the daughter board. Using this socket, several of the key signals to and from the CPU can be easily obtained.

The next socket that plugs into the TNC is at U18. This used to be one of the 2708 EPROM sockets. This socket is used to recover the latched low-order address bus from the latch (U6) on the Vancouver TNC. It was possible to add another latch on the daughter board, but that would have increased loading on the data bus unnecessarily. In addition, plugging into U18 provides structural support for the VDS-1. Since the socket at U18 is used only as a jumper, there is not an IC that plugs into U18.

The third wire-wrap socket between the two boards is at U9, the I/O port decoder. This socket is used to get the additional port decoder output for the 8253 timer IC at U41. U41 uses ports 28H to 2FH. The IC that was plugged into U9 on the TNC now plugs into the daughter board U9 instead.

The fourth wire-wrap socket is at U11. This position used to have the CD4024 baud rate generator plugged into it. Since the baud rate is now generated by U41, there is no IC plugged into the U11 socket on the daughter board. Note that all the old output pins of the CD4024 are now shorted together, it doesn't matter which switch at S2 is closed, as long as at least one is.

VDS-1 EPROM Memory

The VDS-1 board has four sockets for EPROM use. The types of EPROMs acceptable by the VDS-1 are 2716, 2732, or 2764. All four EPROMs must be of the same type. A new EPROM address decoder is used on the daughter board at U38. The address inputs to U38 come from jumper JP-5. JP-5 is pre-wired for 2732 type EPROM decoding. If EPROMs other than 2732's are to be used, the traces on the back of the VDS-1 must be cut before using JP-5. See the Option Settings section for further details.

Note that all three types of EPROMs usable on the VDS-1 run on +5V only, so the other two voltages used by the 2708 EPROMs are not needed for EPROM use. The -5V is no longer needed at all, so it can be eliminated. The +12V is used by the RS-232 interfaces, so it is still needed. Another advantage of getting rid of the 2708's is that the newer types of EPROMs run at a higher speed, reducing the potential of timing problems.

VDS-1 RAM Circuitry

A separate RAM memory decoder (U39, a 74LS138) is now used on the VDS-1. This allows the RAM chip size to be different than the EPROM, allowing greater system flexibility. Like the EPROM decoder, the RAM decoder address inputs come from a jumper (JP-6). This jumper is pre-wired for 6116 type devices. Optionally, 6264 or 2186 type (8k by 8) devices can be used, if JP-6 is altered. Since the 2186 is a psuedo-static device (it is really dynamic, but all support circuitry is inside the chip), it needs to tell the CPU whenever it is not ready. This is why the jumpers JP-9 thru JP-12 are needed. They allow the RAM chips to tell the CPU when they are not ready yet, and the CPU adds wait states until the RAM chips are ready.

VDS-1 Timing Circuitry

One of the problems with the original Vancouver TNC is that the user must change switches to alter the baud rate of the packet channel. In addition, the slowest speed the TNC board runs without modification is 600 baud. This is still too fast for HF packet operation at the moment. The VDS-1 removes this problem by replacing the CD4024 binary counter and S2 with a programmable timer IC (U41, an 8253). The 8253 has three separate programmable timers, one of which is used to create the clock for the 8273 Protocol Controller. Unfortunately, the 8253 can only handle input clock speeds up to 2 MHz. The TNC board's clock is divided by two by U40 on the daughter board (the now famous CD4024) which is then sent to the 8253 timer 0 clock input. The output of timer 0 is then sent to the wire-wrap socket at U11, which feeds it to the TNC board.

A second output of the CD4024 is used to drive the 8253 input clock for timers 1 and 2. These timers are optionally used to drive the trap (non-maskable) and INTR (maskable) interrupt inputs to the 8085 CPU. Since the outputs of the timers are active low, they must be inverted before sending them to the CPU. This inversion is accomplished by U42, a 74LS00. This IC was left over from the original Vancouver TNC memory decoder. If timed interrupts are not being used, they should be disabled by removing U42.

Jumper JP-7 is provided to allow the user to alter the standard input clock rates to the 8253 timer. It is not anticipated that these need to be changed, so JP-7 is normally not altered.

Note that if timers 1 or 2 are used to generate timed interrupts, they must be programmed for a short duration pulse, since the TRAP and INTR interrupts are level sensitive, and will continue to interrupt as long as the inputs are high.

TROUBLESHOOTING

Since the Vancouver TNC is a complete microcomputer system, it can be very difficult to correct problems that may arise. If there is a problem, use the following steps as a guideline to troubleshoot the TNC system. It is helpful to have another TNC board available for comparing, and also for chip swapping.

Certain of the following steps can be ignored if that part of the board seems to be functioning. If, for example, the board works with the terminal, but will not transmit or receive over the packet channel, the whole TNC is not defective, but rather just the HDLC controller or its support circuitry. The following steps are more to help when the whole TNC seems to be out-to-lunch.

Step 1. Overall Tests

A. Make sure that all chips on the TNC are positioned properly. The TNC board has several chips in different orientations, so it is easy to put a chip in backwards. Also make sure that none of the pins on the chips is bent under rather than in the socket hole. This can be done by looking carefully down the end of each socket. If a pin is bent under, remove the chip, bend the pin back, and re-install the chip.

B. If the TNC functions properly until it tries to transmit, then either sends a steady tone, of continual flags (the eternal frame syndrome), replace the CD4024, and try again. This chip is EXTREMELY sensitive to static, and is the number one cause of TNC malfunctions that AMRAD has encountered.

C. Check the power supply lines, both with a meter AND a scope. Three terminal regulators have a habit of going into oscillation, which won't show up on a meter.

D. Check the TNC system with a monitor ROM that is known to work. Sometimes EPROMs forget a bit here or there, causing strange results.

E. Double check the jumpers on both boards. It is not immediately obvious what the proper jumper configuration on the Vancouver TNC board should be in all cases.

F. Remove the daughter board and re-install the ICs removed from the TNC. Try bringing up the TNC without the daughter board to identify where the problem is, preferably using a monitor program in a 2708 and RAM at 1000H-1FFFH. If the TNC functions normally, proceed to step 3, VDS-1 Troubleshooting.

Step 2. Vancouver Board Troubleshooting

A. Apply power to the TNC board. Using a scope, check pin 37 of U1 for a 2.4576 MHz clock. The actual frequency is not important at this time, as long as it is a nice, clean square wave. If not, try installing a couple 20pf capacitors from U1 pins 1 and 2 to ground. Sometimes the 8085 needs these capacitors to function properly. If that doesn't correct the problem, replace the 8085 (U1), and then the crystal if still no clock.

B. Push the Reset button. As long as the button is held down, U1 pin 36 should be low, and U1 pin 3 should be high. The following should also be true as long as reset is held down:

1) Data lines (pins 12-19) should be high.
2) Address lines (pins 21-28) should be 1V. or less.
3) Pins 31, 32, and 35 should be held high.
4) Pins 30, 34, 6, and 10 should be low.
5) Pins 7, 8, and 9 should be low, depending on other chips.

C. Consult your schematic if one of these pins is not at the proper level, and look over the TNC board for shorts.

D. Release the Reset button. U1 pin 36 should now go high, and pin 3 should go low. The following should also be checked (since the address and data buses are not buffered, these signals will not be ideally shaped pulses):

1) Data lines should have alternating high-low pulses.
2) Address lines should have alternating ihgh-low pulses.
3) Check the output pins of the address latch (U6) to make sure it is latching the low-half address properly.
4) Make sure the pins 30, 31, 32, and 34 also have pulses when they are supposed to.
5) Type characters on the console (assuming a serial interface) and look for U1 pin 9 (RST5.5) to go high on each keystroke.

E. Check for active-low transitions on the chip select pins of at least the low EPROM (U15 pin 20). There should also be intermittent transitions on the RAM chip select lines, depending on the program being run.

F. If nothing obvious has ben found at this point, usually the next step is to start swapping chips between a functional TNC and the defective board. If all the chips have been changed, and the board still fails to operate, it is time to check the board with a meter for shorts or bad sockets.

Step 3. Daughter Board Troubleshooting

Note that all pin numbers for EPROM and RAM chips mentioned below (except for U18) are assuming 28 pin sockets, since that is what the daughter board is layed out for. Take this into account when testing 24 pin devices in the 28 pin sockets.

A. Most problems associated with the daughter board have to do with the interconnections between it and the TNC board. Make sure once again that all sockets are soldered properly, and that all the pins line up in the proper holes.

B. Remove U42, if installed. This will make sure no spurious interrupts are being generated by the 8253 timers. U42 should be installed ONLY if software is included to support timed interrupts.

C. Make sure that all the jumpers on the daughter board are correct for the type of memory being used. The VDS-1 is normally jumpered for 2732 EPROMs and 6116 RAMs. See the Options Setting section for more information.

D. Follow A through D in Step 2 above. Perform the tests first on the 8085 itself, then on the bottom of the TNC board's U1 socket to make sure all the signals are making it through the jumpers ok.

E. Check U18 pins 1 to 8 to make sure all bits of the low-order address bus are getting from the TNC to the daughter board.

F. Check the output of the address decoders. At a minimum, U30 pin 20 (EPROM 0 chip select) should be periodically pulsing low. In addition, U34 pin 20 should also be pulsing low, depending on the software being used.

G. As with the TNC board itself, the easiest method to proceed at this point is to swap all ICs on the daughter board with one that is functional (it might be good to try the other daughter board first). If problems persist, carefully go over the daughter board for shorts of bad solder joints.

SOFTWARE SUPPORT

There are a few modifications that must be made to any software before running it on a Vancouver TNC with the VDS-1 installed. These have to do with larger EPROM space, relocated and larger RAM, software control of the packet channel speed, and optionally timed interrupts.

EPROM SUPPORT

Actually, no changes need to be made for the EPROM space itself, but the additional EPROM space means that all RAM location equates need to be changed.

RAM SUPPORT

Most of the programs written for the Vancouver TNC use two equates for the RAM, one for the beginning and the other end of RAM memory. All other references to RAM memory locations are made based on these two equates. When using the VDS-1, all RAM starts at location 8000H. Using four 6116 type RAM chips, RAM will end at 9FFFH. This means the two equates are now as follows:

```
LORAM     EQU  8000H      ; Start of RAM memory
HIRAM     EQU  9FFFH      ; End of RAM memory
```

In addition, two other equates must be changed in the LIPM.ASM file to make it work properly. The order of these equates is now reversed, and they MUST be in this sequence:

```
LBALEN    EQU  (HIRAM-LBA)/2   ; LENGTH OF LINE BUFFER AREA
LBAEND    EQU  (LBA+LBALEN)    ; NEXT BYTE AFTER LINE BUFFER
```

TIMER SUPPORT

Since the packet channel baud rate is now controlled by software, some software must be provided to set the packet speed. In addition, the timer must be initialized before any speed can be selected. The most rudimentary form of code to do these functions at 1200 baud is as follows:

```
CTR0      EQU  28H  ; COUNTER 0 PORT
CTR1      EQU  29H  ; COUNTER 1 PORT
CTR2      EQU  2AH  ; COUNTER 2 PORT
CTRPRM    EQU  2BH  ; COUNTER PARAMETER PORT

CTRIN:    MVI  A,36H     ; CTR0, SQUARE WAVE, BINARY MODE
          OUT  CTRPRM    ; SEND IT TO THE PARAMETER PORT
          MVI  A,20H     ; LOW HALF DIVIDER FOR 1200 BAUD
          OUT  CTR0      ; SEND LOW HALF TO COUNTER 0
          MVI  A,0       ; HIGH HALF DIVIDER 0
          OUT  CTR0      ; AND SEND IT TO COUNTER 0
```

SOFTWARE SUPPORT (CONTINUED)

The following is some information on programming the 8253 chip. It is given in assembly format to aid in installing it in software.

```
CNTR02    EQU  80H  ; SELECT COUNTER 2 FOR PROGRAMMING
CNTR01    EQU  40H  ; SELECT COUNTER 1 FOR PROGRAMMING
CNTR00    EQU  00H  ; SELECT COUNTER 0 FOR PROGRAMMING
RDLDBH    EQU  30H  ; READ/LOAD LOW BYTE FIRST, THEN HIGH
                    ; OF DIVIDER IN COUNTER SPECIFIED
RDLDHI    EQU  20H  ; READ/LOAD HIGH BYTE ONLY OF DIVIDER
RDLDLO    EQU  10H  ; READ/LOAD LOW BYTE ONLY OF DIVIDER
CNTLAT    EQU  00H  ; LATCH THE COUNTER AT PRESENT COUNT
MODE05    EQU  0AH  ; MODE 5 (HWARE TRIGGERED STROBE)
MODE04    EQU  08H  ; MODE 4 (SWARE TRIGGERED STROBE)
MODE03    EQU  06H  ; MODE 3 (SQUARE WAVE GENERATOR)
MODE02    EQU  04H  ; MODE 2 (PULSE RATE GENERATOR)
MODE01    EQU  02H  ; MODE 1 (PROGRAMMABLE ONE-SHOT)
MODE00    EQU  00H  ; MODE 0 (INTERRUPT ON TERMINAL CNT)
BCDCNT    EQU  01H  ; BCD COUNTER MODE (4 DECADES)
BINCNT    EQU  00H  ; BINARY MODE (16 BITS).
```

It should be noted that each counter is programmed via the control port, and that the actual counter ports are used only for loading or reading the count of the timer.

Consult the Intel 8253 data sheets for more information on programming the 8253.

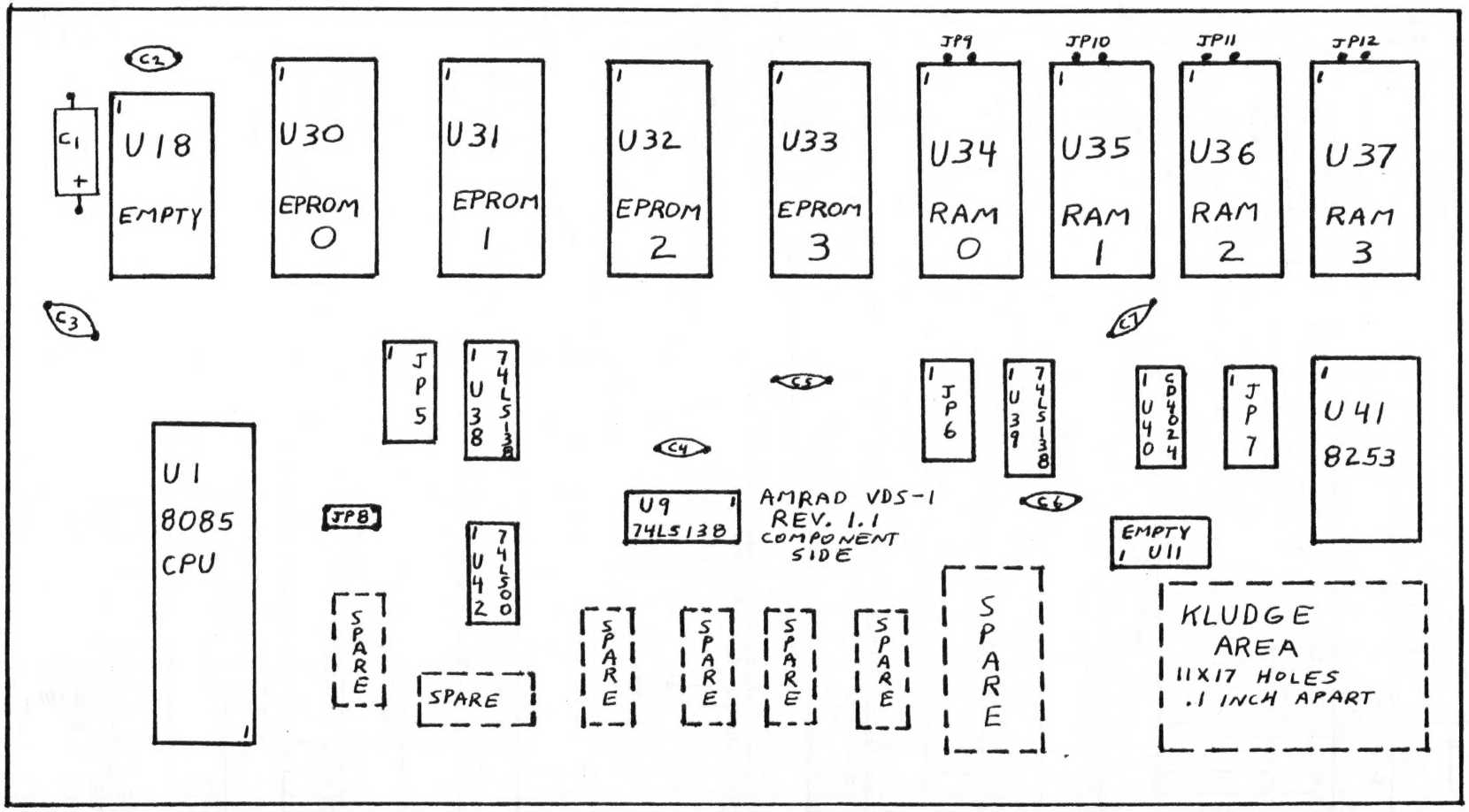
The next table contains the BINARY divider to load into the 8253 timer 0 for most common baud rates.

SPEED	Low Half Divider	High Half Divider
9600	04H	00
4800	08H	00
2400	10H	00
1200	20H	00
600	40H	00
300	80H	00
150	00H	01H
75	00H	02H

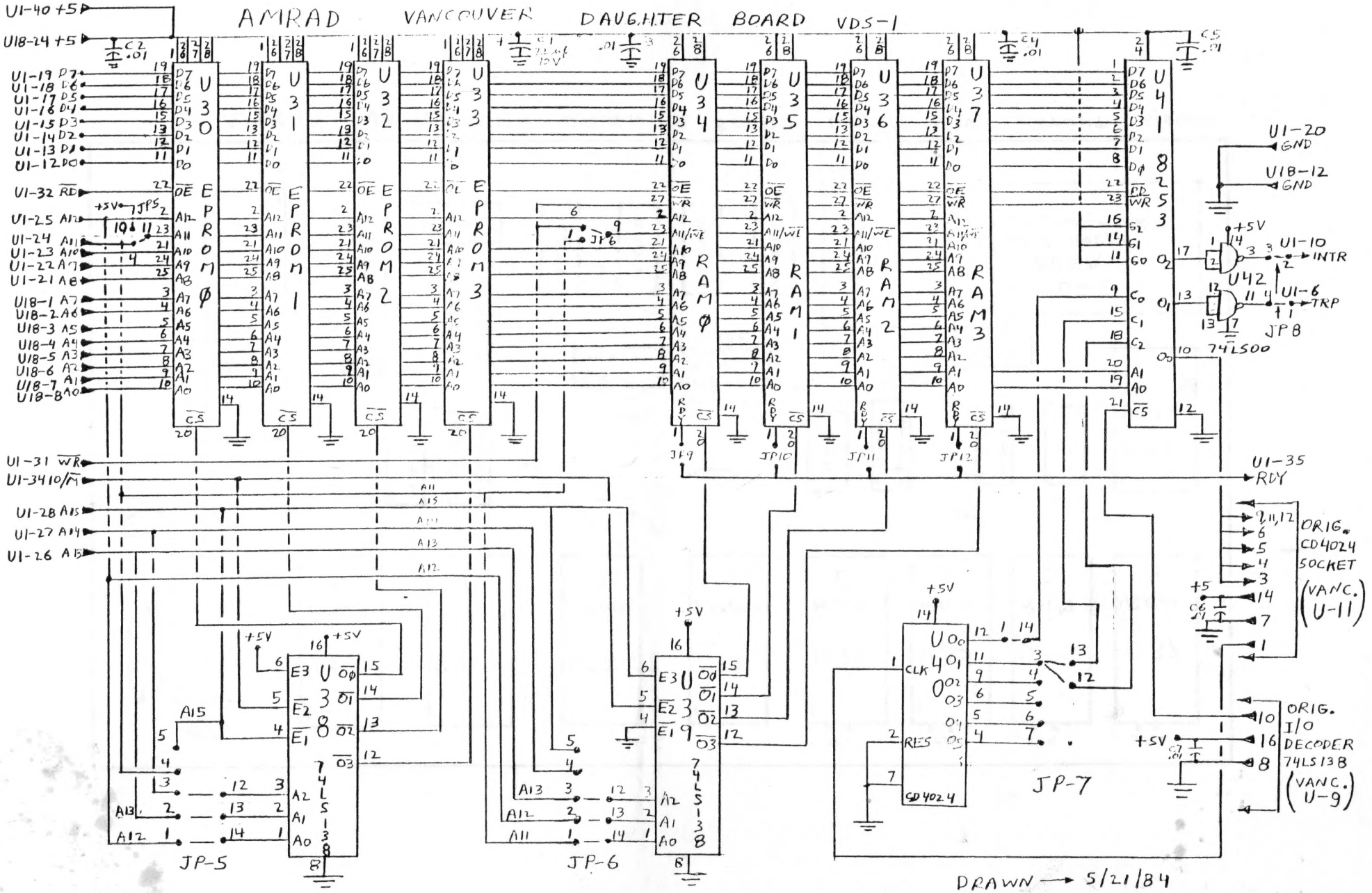
VDS-1 PARTS LIST

The following is a list of parts necessary for the construction of the AMRAD VDS-1 Daughter Board.

QUANTITY	PART NUMBER	DESCRIPTION
1	VDS-1	AMRAD Daughter PC Board.
1	74LS138	1 of 8 Decoder IC
1	8253	Programmable Interval Timer IC
1-4	2716,2732,2764	EPROM Memory IC (depending on size)
1-4	6116,6264,2186	RAM Memory IC (depending on size)
1	40 Pin Wire-Wrap	IC Socket
1	24 Pin Wire-Wrap	IC Socket
1	16 Pin Wire-Wrap	IC Socket
1	14 Pin Wire-Wrap	IC Socket
8	28 Pin Solder-Tail	IC Socket (optionally 4 Solder-Tail and 4 ZIF sockets for EPROMs)
1	24 Pin Solder-Tail	IC Socket
2	16 Pin Solder-Tail	IC Socket
2	14 Pin Solder-Tail	IC Socket
3	14 Pin Solder-Tail	IC Socket (Options)
3	14 Pin DIP Headers	(Options)
1	47uF 10V Electrolytic Capacitor	(value not critical)
6	.1uF 50V Disc Capacitor	



AMRAD VANCOUVER DAUGHTER BOARD COMPONENT LAYOUT 6/30/84


AMRAD VANCOUVER DAUGHTER BOARD VDS-1
U1-40 +5
U18-24 +5
U1-19 D7
U1-18 D6
U1-17 D5
U1-16 D4
U1-15 D3
U1-14 D2
U1-13 D1
U1-12 D0
U1-32 RD
U1-25 A12
U1-24 A11
U1-23 A10
U1-22 A9
U1-21 A8
U18-1 A7
U18-2 A6
U18-3 A5
U18-4 A4
U18-5 A3
U18-6 A2
U18-7 A1
U18-8 A0
U30 EPROM 0
U31 EPROM 1
U32 EPROM 2
U33 EPROM 3
U34 RAM 0
U35 RAM 1
U36 RAM 2
U37 RAM 3
U41 8253
U42 74LS00
JP5
JP6
JP7
JP8
JP9
JP10
JP11
JP12
U1-31 WR
U1-34 IO/M
U1-28 A15
U1-27 A14
U1-26 A13
U1-35 RDY
U1-20 GND
U18-12 GND
U1-10 INTR
U1-6 TRP
ORIG. CD4024 SOCKET (VANC. U-11)
ORIG. I/O DECODER 74LS138 (VANC. U-9)
CD4024
74LS138
DRAWN → 5/21/84
LATEST REVISION 1.1 DATE: 6/30/84
BY TERRY FOX, WB4JFI